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Three-level PN cell for multilevel converters

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Abstract:
Multilevel converters rely on plurality of DC capacitors switched in specific patterns to obtain the necessary output voltage level. MMC, FLC and NPC converters require complex control to balance the capacitors' voltages. CHB converters require plurality of isolated DC sources to energize the capacitors. This paper presents a three-level PN cell that modulates the common-mode voltage between the output and input port while simultaneously mirroring the input DC voltage on the output port. Cell's capacitor voltage is naturally balanced and a three-phase multilevel converter requires only one DC power source. The output voltage of a multilevel converter can be higher than the input DC voltage. As a consequence a single low voltage DC power source can directly interface a three phase MV grid.

1 Introduction

Medium and high voltage power electronics is commonly used in industrial applications such as power transmission, oil and gas, traction, marine propulsion and process industries [1–4]. All these industries operate power converters in the MVA power range. For a long time the designs were limited by the breakdown voltage levels of available semiconductors, a situation that is slowly changing due to recent availability of high blocking voltage devices [5]. Multilevel level topologies (e.g. NPC, FC and CHB) were introduced to increase the system voltage level while still using the LV semiconductors and to increase the number of possible voltage levels thus making the output voltage more closely resemble sinusoidal waveform [6]. This, in turn, means the output filter could be made smaller promising a smaller total system form factor. Despite these benefits, these topologies never reached substantial market penetration.

The situation changed with the introduction of modular multilevel converters (MMC) [7]. Their modular nature allows a high number of output voltage levels and provides redundancy at a cost of a complex control [8, 9]. Most of the multilevel topologies rely on plurality of DC sources switched in a specific way to obtain a desired output voltage. NPC and CHB topologies require isolated or stacked DC voltage sources which are not easily obtainable. FC and MMC topologies generate the required voltage sources by charging DC capacitors to a required voltage level and rearranging their connection to achieve the desired output voltage.

The inherent problem in this approach is that the capacitors require complex strategies to keep them charged at a desired DC voltage level [10–13]. Charging/discharging pattern is typically limited by modulation requirements therefore the required capacitance value is strongly tied to the output current magnitude and frequency. Low line frequency (50/60Hz) and high current magnitudes required in the applications where these converters are typically used require very high capacitance values [14].

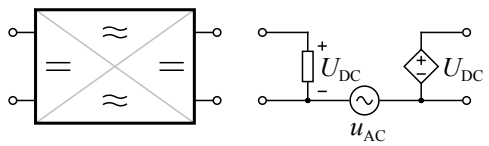

Fig. 1: Proposed symbol for a converter cell and its simplified electrical model. Input and output ports are DC ports, output voltage has the same magnitude as input voltage. The converter modulates the common mode voltage u_{AC}.

In this paper we present a three-level converter PN cell with inherent capacitor voltage balancing mechanism. Its topology is closely related to cascaded H-bridge converter and also switched capacitor converters which are most often used for LV high integration scale.

$$\bar{u}_{\mathrm{AC}} = m\,U_{\mathrm{DC}}\sin(\omega t) \tag{1}$$

Fig. 1 shows a simplified electrical model of the proposed converter as well as proposed cell symbol. The converter cell modulates the common mode voltage between output and input port (eq. 1) while preserving the DC voltage magnitude between the two ports.

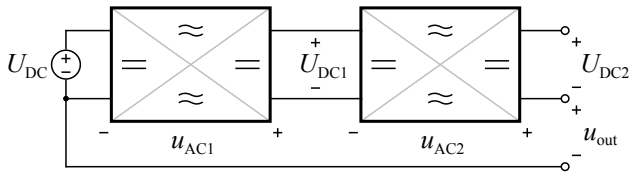

Fig. 2: Block diagram of a single-phase five-level converter composed of two three-level modules.

Because the DC voltage applied to the input is reflected on the output port, the converter can be easily daisy-chained, as shown in fig. 2, where $U_{\mathrm{DC}} = U_{\mathrm{DC1}} = U_{\mathrm{DC2}}$ (this is a simplification, full explanation follows in section 2.4). Each cell contains a capacitor for energy storage across the output port of the cell. The capacitor cell voltage is naturally balanced to the cell input voltage thus complex capacitor voltage balancing schemes are not necessary.

The converter output voltage is the sum of common mode voltages $u_{\mathrm{AC}n}$ generated by individual converter cells. For a converter with two daisy-chained cells the output voltage is

$$u_{\mathrm{out}} = u_{\mathrm{AC1}} + u_{\mathrm{AC2}} \tag{2}$$

and has $2n+1$ discrete levels, where n is the number of daisy-chained converter cells.

A key observation from eq. 1 and eq. 2 is that the output voltage can have a higher magnitude than the input DC voltage and can be increased even further by adding more converter cells. This may allow e.g. a LV DC generator interface a MV grid without a step-up transformer.

$$u_{\mathrm{out}} = n \cdot m\,U_{\mathrm{DC}}\sin(\omega t) \tag{3}$$

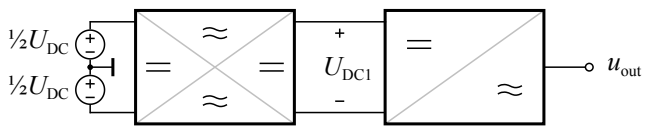

Fig. 3: Block diagram of a single-phase four-level converter composed of and three-level module and a one two level converter.

Finally, because the DC voltage is preserved throughout the converter chain, there is a possibility of placing a classical two-level half-bridge at the end of the chain, as in fig. 3. This increases the number of output voltage levels to $2n + 2$ by adding only two transistors.

The aforementioned properties: ease of daisy-chaining the converter cells, natural cell capacitor voltage balancing and ability to connect a LV DC source directly to a MV grid are key properties of the presented PN converter cell and multilevel converters based on it.

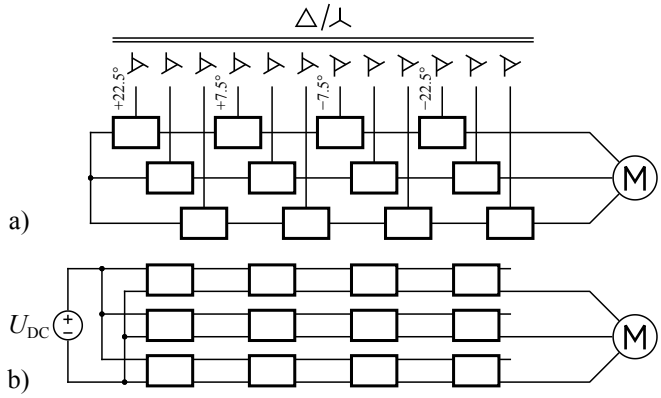

Fig. 4: Three-phase nine-level MV converters:
a an industrial implementation of a CHB topology;
b converter built using the proposed PN cells.

One important application of this topology is in MV drives. In an industrial MV CHB drive converter the power is delivered to the cells using a multiple output transformer as in fig. 4a [15]. In this embodiment the secondary windings of the transformer are phase shifted to maximise the input power quality. One disadvantage of this approach is that the transformer is relatively large and complex. The transformer needs to be redesigned if different power level or number of cells are used. Moreover, each power cell needs a rectifier on the transformer input port.

In a PN cell based converter (fig. 4b) the power is sourced from a single DC source and distributed to the cells using daisy-chaining. The single DC power source can be implemented using any standard LV topology and the power level can be easily adjusted by paralleling. The converter can be easily interfaced to existing DC microgrids, e.g. in marine applications where a low or medium voltage DC grid distributes power to propulsion and individual thrusters.

Another possible application of the presented PN cell based converters is in wind power converters where the LV generator can be directly connected to a MV collection grid removing the need for bulky LV cables and transformer thus lowering the total weight of the structure. Similarly, the converter can be used in PV applications where it can interface a string of PV panels to the AC grid.

The main objective of this paper is to introduce the PN converter cell to the reader and to give insight into design opportunities and challenges when designing multilevel converters using this cell. Section 2 describes the topology and switching states of the proposed cell. It also presents an average model that is then used to investigate basic dynamic behaviour of the cell capacitor voltage. Next, we use two topology case studies to investigate which operating conditions are best suited for the design and which should be avoided. Finally, we present a derived simplified topology that minimises the number to transistors needed in a converter cell. In section 3 we discuss issues of scalability. We present experimental work used that was done to demonstrate the concept of the PN converter cell in section 4. Afterwards, in section 5, we present related work that was used as an inspiration for this paper.

2 Multilevel converter cell

2.1 Converter cell topology

The proposed power cell is derived from a cascaded H-bridge topology [15]. In the CHB topology, individual cells are daisy chained in a string as shown in fig. 5a. The energy in the cell is typically sourced from a isolated AC source, such as a transformer, and rectified in the cell. Each cell requires an isolated power source therefore a single input multiple output transformer is typically used.

In contrast, the PN-cell based topology does not require isolated power sources. The power is transferred from one cell to the next by additional transistors joining the adjacent cells as show in fig. 5b.

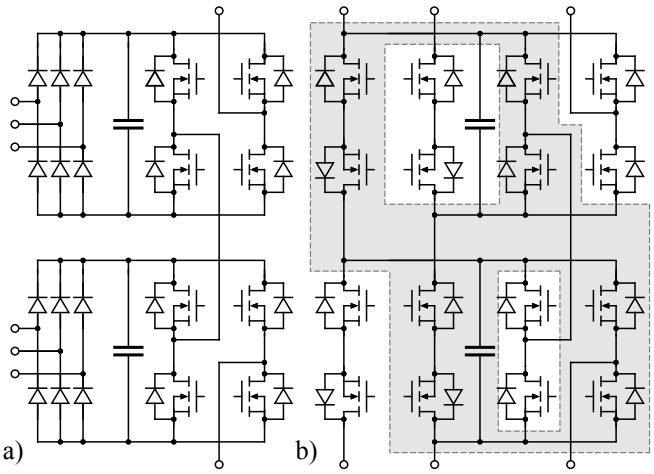

Fig. 5: Part of a converter chain in
a cascaded H-bridge topology;
b PN-cell based topology, greyed area shows the cell boundary.

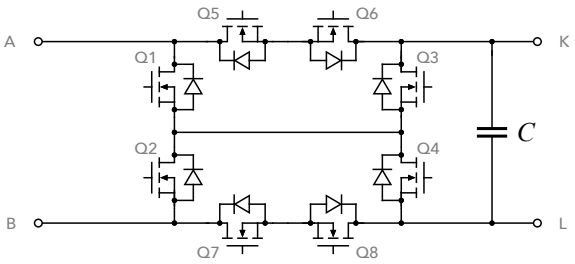

Fig. 6: Schematic diagram of a single converter cell.

A single PN converter cell circuit, redrawn in fig. 6 to simplify the understanding of the cell operation, is a two port network with eight transistors and an energy storage cell (capacitor or a battery) on the output port. Under ideal operation the magnitudes of U_{AB} and U_{KL} voltages are equal and constant. The converter modulates the common mode voltage of the secondary side with respect to the primary side. The modulated common mode voltage is effectively seen as AC voltage on ports LB and KA.

Standard multilevel flying capacitor (FC) topologies require the capacitors to be pre-charged to a specified voltage. The voltage on the capacitors then needs to be actively balanced to ensure proper

operation of the converter [16]. In the proposed converter topology, the cell capacitor voltage is reset to its nominal DC voltage by connecting the cell capacitor to the cell input port (which is either the capacitor of the previous cell or DC voltage source at the beginning of the converter chain).

2.2 Switching states

The converter cell is comprised of eight switches. The switches connecting the primary (AB) and secondary (KL) DC sides operate effectively as four quadrant switches $Q_5 = Q_6$ and $Q_7 = Q_8$. Switches on the DC ports operate complementarily, therefore $Q_1 = \bar{Q}_2$ and $Q_3 = \bar{Q}_4$ which reduces the number of independent switches to four. Fig. 7 and table 1 summarises the switching states of the converter cell. During the zero state, the cell capacitor is connected to the cell input terminal, equalising the u_{AB} and u_{KL} voltages.

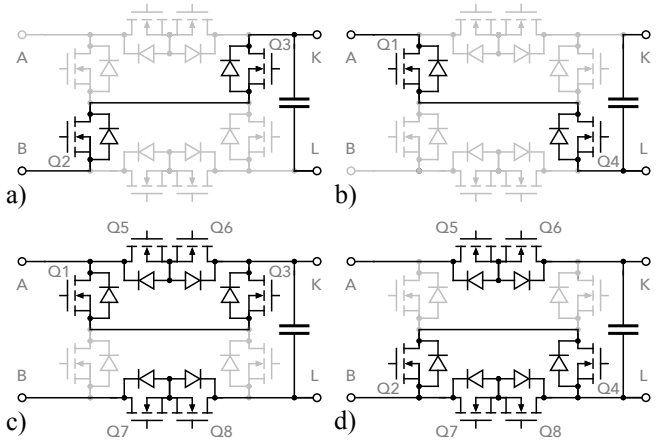

Fig. 7: Switching states for generating:
a negative (N);
b positive (P);
c,d zero common voltage (0).
Note: not all zero voltage switching states are shown.

2.3 Average model

A multilevel power converter contains high number of transistors which typically leads to substantial simulation times. In order to speed up the simulations an average model of the converter cell can be used. The model will also aid in explanation of the dynamics inside a converter chain built from plurality of the presented cells.

Following table 1, the converter cell can be represented as three different equivalent circuits, as seen in fig. 8. Transistor resistances are bundled into effective resistances R_{P}, R_{N}, $R_{0\mathrm{H}}$ and $R_{0\mathrm{L}}$. The value of zero state resistances depends on the specific zero state used in the modulator. $d_{\mathrm{P}} = t_{\mathrm{P}}/t_{\mathrm{SW}}$, $d_0 = t_0/t_{\mathrm{SW}}$ and $d_{\mathrm{N}} = t_{\mathrm{N}}/t_{\mathrm{SW}}$ where $d_{\mathrm{P}} + d_0 + d_{\mathrm{N}} = 1$. $u_{\mathrm{C}} = u_{\mathrm{KL}}$.

Table 1 Switching states for the converter cell.

State	u_{LB}	$Q_1 = \bar{Q}_2$	$Q_3 = \bar{Q}_4$	$Q_5 = Q_6$	$Q_7 = Q_8$
P	U_{AB}	1	0	0	0
0	0	0	0	1	1
		0	0	1	0
		1	1	1	1
		1	1	0	1
N	$-U_{\mathrm{KL}}$	0	1	0	0

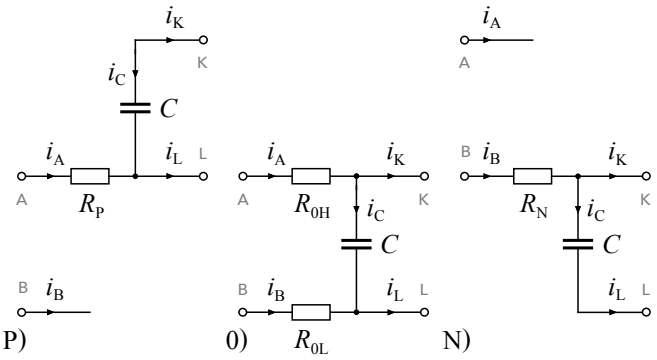

Fig. 8: Equivalent converter cell circuits for positive, zero and negative switching states (P, 0 and N respectively).

$$C\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t} = \begin{cases} -i_{\mathrm{K}} & \text{for } d_{\mathrm{P}} \\ \dfrac{u_{\mathrm{AB}} - u_{\mathrm{C}} - R_{0\mathrm{H}} i_{\mathrm{K}} + R_{0\mathrm{L}} i_{\mathrm{L}}}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} & \text{for } d_0 \\ i_{\mathrm{L}} & \text{for } d_{\mathrm{N}} \end{cases} \tag{4}$$

$$C\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t} = d_0 \frac{u_{\mathrm{AB}} - u_{\mathrm{C}} - R_{0\mathrm{H}} i_{\mathrm{K}} + R_{0\mathrm{L}} i_{\mathrm{L}}}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} - d_{\mathrm{P}} i_{\mathrm{K}} + d_{\mathrm{N}} i_{\mathrm{L}} \tag{5}$$

$$u_{\mathrm{LB}} = \begin{cases} u_{\mathrm{AB}} - R_{\mathrm{P}}(i_{\mathrm{K}} + i_{\mathrm{L}}) & \text{for } d_{\mathrm{P}} \\ \dfrac{R_{0\mathrm{L}}\left(u_{\mathrm{AB}} - u_{\mathrm{C}} - R_{0\mathrm{H}}(i_{\mathrm{K}} + i_{\mathrm{L}})\right)}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} & \text{for } d_0 \\ -u_{\mathrm{C}} - R_{\mathrm{N}}(i_{\mathrm{L}} + i_{\mathrm{K}}) & \text{for } d_{\mathrm{N}} \end{cases} \tag{6}$$

$$u_{\mathrm{LB}} = d_{\mathrm{P}}\big(u_{\mathrm{AB}} - R_{\mathrm{P}}(i_{\mathrm{K}} + i_{\mathrm{L}})\big) - d_{\mathrm{N}}\big(u_{\mathrm{C}} + R_{\mathrm{N}}(i_{\mathrm{K}} + i_{\mathrm{L}})\big) + \\ + d_0 \frac{R_{0\mathrm{L}}\left(u_{\mathrm{AB}} - u_{\mathrm{C}} - R_{0\mathrm{H}}(i_{\mathrm{K}} + i_{\mathrm{L}})\right)}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} \tag{7}$$

$$i_{\mathrm{A}} = \begin{cases} i_{\mathrm{K}} + i_{\mathrm{L}} & \text{for } d_{\mathrm{P}} \\ \dfrac{u_{\mathrm{AB}} - u_{\mathrm{C}} + R_{0\mathrm{L}}\left(i_{\mathrm{K}} + i_{\mathrm{L}}\right)}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} & \text{for } d_0 \\ 0 & \text{for } d_{\mathrm{N}} \end{cases} \tag{8}$$

$$i_{\mathrm{A}} = d_{\mathrm{P}}\left(i_{\mathrm{K}} + i_{\mathrm{L}}\right) + d_0 \frac{u_{\mathrm{AB}} - u_{\mathrm{C}} + R_{0\mathrm{L}}\left(i_{\mathrm{K}} + i_{\mathrm{L}}\right)}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} \tag{9}$$

$$i_{\mathrm{B}} = \begin{cases} 0 & \text{for } d_{\mathrm{P}} \\ \dfrac{u_{\mathrm{C}} - u_{\mathrm{AB}} + R_{0\mathrm{H}}\left(i_{\mathrm{K}} + i_{\mathrm{L}}\right)}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} & \text{for } d_0 \\ i_{\mathrm{K}} + i_{\mathrm{L}} & \text{for } d_{\mathrm{N}} \end{cases} \tag{10}$$

$$i_{\mathrm{B}} = d_0 \frac{u_{\mathrm{C}} - u_{\mathrm{AB}} + R_{0\mathrm{H}}\left(i_{\mathrm{K}} + i_{\mathrm{L}}\right)}{R_{0\mathrm{H}} + R_{0\mathrm{L}}} + d_{\mathrm{N}}\left(i_{\mathrm{K}} + i_{\mathrm{L}}\right) \tag{11}$$

All of the equations have been implemented in LTSpice [17]. To verify the average model, we tested it against a switching model of the converter cell in two circuit configurations. More important, these configurations also demonstrate the basic dynamic phenomena and behaviour of the converter cells.

2.4 Converter cell dynamics

We chose two converter circuit topologies to present the basic dynamic properties of the multilevel converter cell. The first circuit is a single cell (three level converter). This shows an operation where there is no current on the K terminal of the cell. The second topology is a four level converter, as shown in fig. 3, where a two level converter is daisy chained after a three level cell. This shows an operation where the 3L cell is not the last element in the chain converter.

To make the cases comparable an AC current source with phase offset with respect to cell output voltage is used. This kind of load represents a RL load and it keeps the current value constant, irrespective of the applied voltage. The input voltage to the converter chain is kept at 400V for both cases. Triangle carrier based PWM with open loop control is used throughout this subsection.

2.4.1 Three level converter: a single converter cell is driving an RL load connected between the L and B terminals.

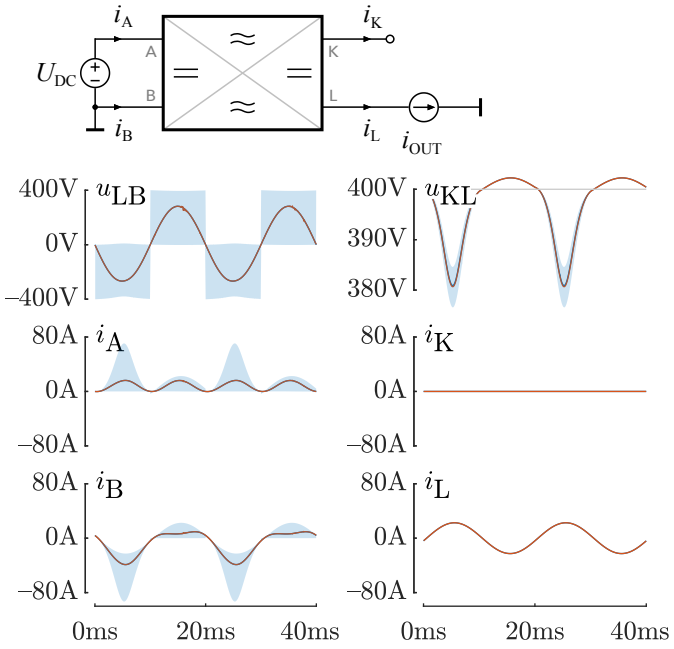

Fig. 9: Sample waveforms three level converter. Average model waveforms (solid line) superimposed on instantaneous waveforms.

The most important observation from fig. 9 is that the capacitor voltage u_{KL} in the cell is not constant. It is an inherent property of this converter cell topology. There are two causes for this behaviour and they are diffrent depending on the u_{LB} voltage polarity.

In the positive u_{LB} half cycle, the circuit alternates between P and 0 states. Because in this circuit configuration $i_K = 0$ the capacitor is never discharged by the output current. Moreover, during the zero state, it is charged to u_{AB} voltage offset by the voltage drops on the zero state resistances R_{0H} and R_{0L}. This causes the voltage on the cell capacitor to temporarily increase above its nominal value.

The explanation behind the exact behaviour in the negative u_{LB} half cycle is more nuanced. In order to keep the voltage constant, the average capacitor current in one switching cycle would need to be zero. Following eq. 5 we can see that i_C is dependent on output port currents (i_K and i_L), resistances in the zero state (R_{0H} and R_{0L}), and on state timings (d_P, d_0 and d_N). As state timings are externally controlled to generate the desired u_{LB} voltage and output port currents are load dependent, the only variable we can use to limit the capacitor voltage variations are the zero state resistances.

Converter cell capacitor's current and voltage at different levels of zero state resistances can be compared in fig. 10. The capacitor charging current is limited only be these resistances. Decreasing the resistances lowers the average voltage swings of the capacitor voltage

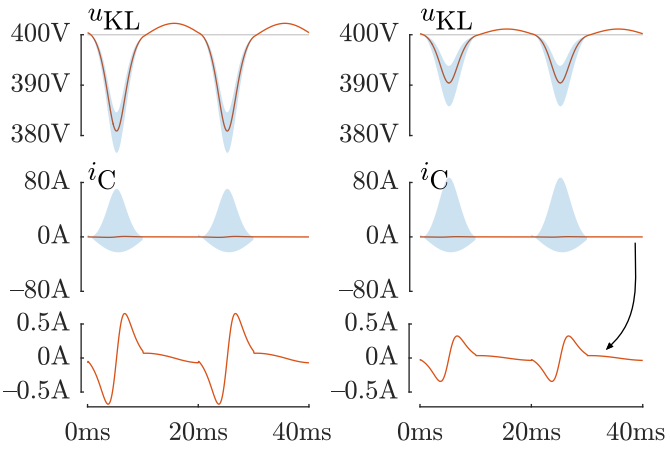

Fig. 10: Qualitative impact of zero state resistances (R_{0H} and R_{0L}) values on cell capacitor voltage and current. Resistances halved on the right plots compared to the left plots. Average model waveforms (solid line) superimposed on instantaneous waveforms.

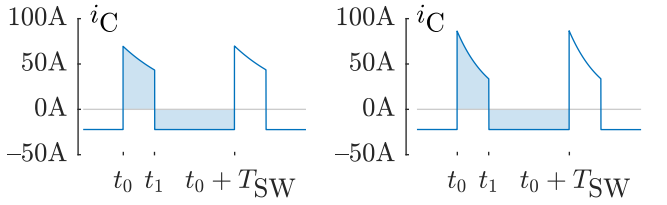

Fig. 11: Qualitative impact of zero state resistances (R_{0H} and R_{0L}) values on cell capacitor voltage and current on a T_{SW} time scale. Resistances halved on the right plot compared to the left plot.

but increases the peak current in the cell as in fig. 11. The zero state resistances are determined only by the choice of the semiconductors therefore the choice should be done with typical operating range in mind. It is the desired resistance value that drives the selection of the semiconductors.

There are several practical limits to the value of these resistances. On the low end the resistance values are limited by conductivity of available semiconductors and peak charging currents that may cause EMC issues. Practically, there is no need for decreasing the resistances below the value at which a capacitor is charged within the t_0–t_1 period. For an RC circuit, after a charging time of three to five τ the circuit is considered fully charged.

$$R_{0H} + R_{0L} > \frac{f_{sw}}{k(1 - m_{max})C}, \text{ where } k \in [3, 5] \qquad (12)$$

From the top, resistance values are limited by the need to charge the cell capacitors to the voltage that is as close to the input port voltage as possible. Bigger resistance values will however decrease the peak to mean ratio of the charging current lowering the stress on the cell capacitors and transistors used in the charging zero state.

The AC component of the cell capacitor voltage impacts the cell output u_{LB} voltage (eq. 7). If the magnitude of this low frequency ripple is much smaller than the DC component in u_{KL} it can be treated as a disturbance in the control circuit. As the frequency of this AC component is the same as the output voltage the converter control algorithm can control this disturbance. However, it must be noted, that the control algorithm will need to increase the modulation index m in order to increase the u_{LB} voltage. Increased modulation index lowers the time in the charging zero state of the cell. Therefore, there exists a limit to the compensation range.

2.4.2 Four level converter: a two level half-bridge is daisy chained to the KL port of a three level converter cell as in fig. 3.

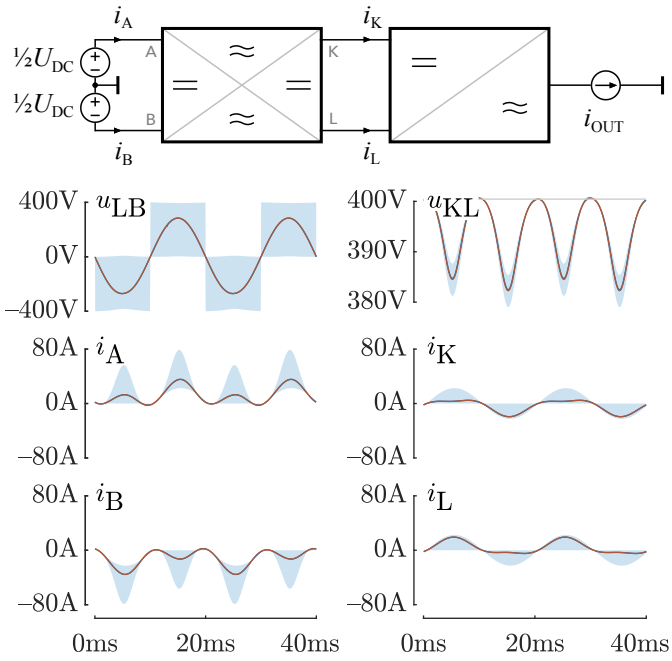

Fig. 12: Sample waveforms four level converter. Average model waveforms (solid line) superimposed on instantaneous waveforms.

Figure 12 shows basic waveforms relating to the three level cell. Contrary to the previous circuit the voltage on the cell capacitor behaves similarly in both the positive and negative output voltage halfcycles.

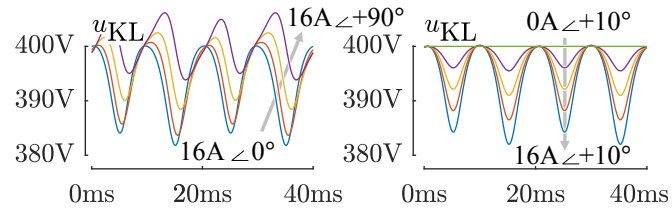

Fig. 13: Impact of load current variation on cell capacitor voltage fluctuations.

To analyse the impact of the load on the oscillations of the cell capacitor voltage two simulations were performed and their results are shown in fig. 13. The magnitude of the load current was held constant and the phase offset of the current to output voltage was adjusted from 0 to 90 degrees emulating a pure resistive to pure inductive loads, respectively. For purely resistive loads the cell capacitor is discharged in both halfcycles of the output voltage. For purely inductive loads the power fluctuates between cell capacitors and load causing positive and negative capacitor voltage swings.

Equation 5 predicts that at high modulation index values, when d_0 time is small, the capacitor current is mostly dependent on the load current. In fig. 14 we can observe the impact of modulation index on capacitor voltage with two different loads: purely resistive and purely inductive. In both cases the peak capacitor voltage drops seem to have a square relationship with modulation index.

In case of purely resistive load and high modulation index ($m = 0.9$), the voltage swing, for this particular converter reaches 15% of nominal capacitor DC voltage. Limiting the modulation index is therefore crucial in minimising the capacitor voltage swings.

For a purely reactive load, cell capacitor voltage swings reach only 3% of the nominal voltage at high modulation index ($m = 0.9$). This happens because the peak load current occurs when the output voltage is close to zero, i.e. when zero vector use is maximised. This observation leads to the conclusion that this topology is especially well

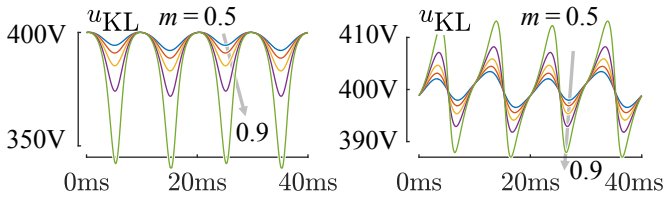

Fig. 14: Impact of modulation index on cell capacitor voltage fluctuations in case of purely resistive load (left) and purely inductive load (right); $I_{\text{load}} = 16A$ for both cases.

suited for reactive power dominant applications, such as STATCOM converters.

The main benefit of this converter compared to a CHB is the size of the capacitors. In a comparative CHB topology the capacitances must be sized to allow the phase current to charge and discharge the cell capacitor while maintaining relatively constant DC voltage on them. This requires very high cell capacitances. In a PN-cell based converters the DC voltage on the capacitor is naturally balanced through modulation therefore smaller cell capacitances are needed. Quantitative analysis of this effect is beyond the scope of the paper as it is very strongly dependent on the specific application and operating point.

2.5 *Derived topologies*

The converter cell presented above has many redundant 0 states. Carefull inspection of table 1 shows that either Q_5 and Q_6 or Q_7 and Q_8 switches can be fixed to zero while maintaining the required common-mode voltage states. The remaining states are depicted in table 2.

Table 2 Simplified switching states from table 1 with $S_7 = S_8 = 0$.

State	u_{LB}	$Q_1 = \bar{Q}_2$	$Q_3 = \bar{Q}_4$	$Q_5 = Q_6$
P	U_{AB}	1	0	0
0	0	0	0	1
N	$-U_{\text{KL}}$	0	1	0

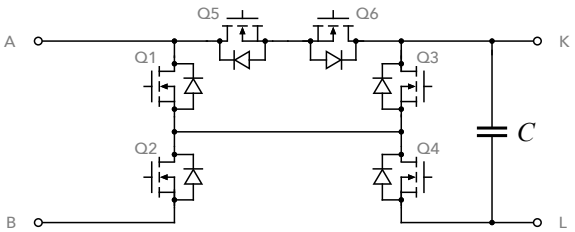

Fig. 15: Schematic diagram of a simplified converter cell.

The original cell structure containing eight transistors (fig. 6), is therefore simplified to use only six transistors, as shown in fig. 15.

The three available switching states from table 2 can be seen as circuit configurations in fig. 16. Removal of Q_7 and Q_8 forces Q_2 and Q_4 transistors to conduct the output capacitor charging current, changing the current stress and loss distribution, compared to the cell with eight transistors. Functionally this modified topology is exactly the same as original one and all average model equations are valid.

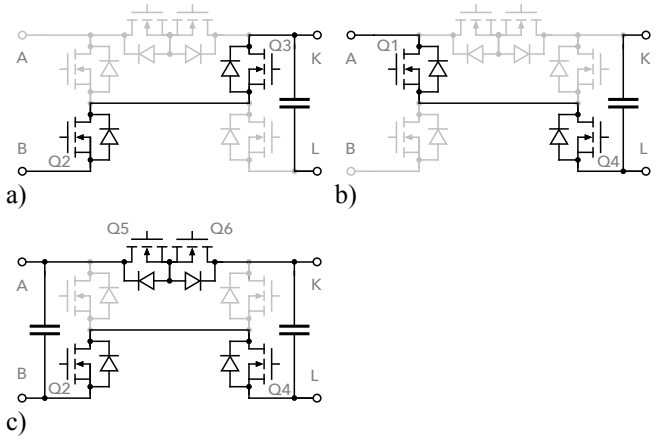

Fig. 16: Switching states for generating:
a negative;
b positive;
c zero common voltage.

3 Converter scalability

This section of work is dedicated to the issues of scalability of a converter built up from described converter cells.

3.1 Power, voltage and current rating

Daisy chaining the converter blocks, as in fig. 2, increases the magnitude of the output voltage and increases the number of possible output voltage levels. The power rating of converter chain blocks is dependent on its position in the chain. A chain block is defined as one cell (or parallel connected cells) generating a single $u_{\mathrm{AC}n}$ voltage.

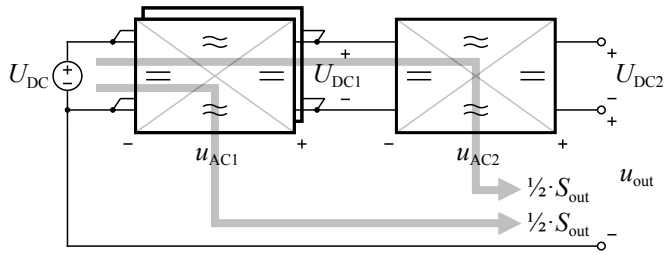

Fig. 17: Power flow in a converter chain. Each arrow represents S_{out}/n power flow.

Assuming output power is S_{out} and each converter chain block generates the same $u_{\mathrm{AC}n}$ voltage equal to u_{out}/n, where n is the number of blocks serialised in the chain, the power delivered to the last block is S_{out}/n while the power delivered to first converter block is equal to S_{out}.

In case of a five level converter with two daisy-chained cells (as in fig. 18), the first chain block must be rated to double the power of the second block. As the DC voltage magnitude is preserved throughout the chain, the block input current varies linearly throughout the chain to reflect the changing input power rating. Individual blocks must be therefore either designed to reflect the different current ratings or can use paralleled converter cells (as in fig. 17) to achieve the desired current rating. The latter solution is practical as only one cell structure needs to be designed.

Consider a system where $S_{\mathrm{out}} = U_{\mathrm{out}} \cdot I^{*}_{\mathrm{out}}$ with n daisy chained blocks delivering $2n + 1$ voltage levels.

$$U_{\mathrm{out(pk)}} = \sqrt{2} \cdot U_{\mathrm{out}} = n \cdot U_{\mathrm{AC(pk)}} = n \cdot m_{\max} \cdot U_{\mathrm{DC}} \qquad (13)$$

The minimum DC input voltage is a function of maximum modulation index, number of daisy chained cells and output voltage level.

$$U_{\mathrm{DC(min)}} = \frac{\sqrt{2} \cdot m_{\max}}{n} U_{\mathrm{out}}. \qquad (14)$$

With modulation limit set to $m_{\max} = 1/\sqrt{2}$ the minimum DC voltage is $U_{\mathrm{DC(min)}} = 2/n \cdot U_{\mathrm{out}}$ which is a good rule of thumb when designing a multilevel converter with these cells.

As the current rating in the chain scales linearly, and cells in the chain can be paralleled to achieve the necessary current rating, the current rating is then defined by the last cell that needs to draw $S_{\mathrm{out}}/(n \cdot U_{\mathrm{DC}})$ current.

A full chain composed of n converter blocks requires $n(n+1)/2$ converter cells. Number of the required cells is a triangular number of blocks in the chain.

3.2 Capacitor cell voltages

Ideally, the input DC voltage would propagate through the converter chain without any alterations. This is however not true because output current discharges the capacitor and there is limited time in a switching period where the capacitors can be recharged. This causes deviations from a true DC value, as shown in the previous section. These deviations will impact the converter output voltage (eq. 7) if not compensated by the control system.

Analysing equation 5 we can see that the cell capacitor voltage is dependent on many parameters, namely u_{AB}, resistances in the cell and output port currents i_{K} and i_{L}. Dependence on the input port voltage u_{AB} causes capacitor voltage swings to propagate throughout the converter chain. The analysis of voltage on individual cell capacitors in a multilevel converter becomes a very complex task.

One simplification can come from equations 4, 8 and 10. Notice that i_{A} and i_{B} cell currents depend on sum of cell output port currents $i_{\mathrm{K}} + i_{\mathrm{L}}$. As the cells are daisy chained the sum of output port currents is therefore always equal to the load current i_{OUT}.

In any case the voltage variations of capacitors across the converter chain are dependent on the position in the chain. Because the capacitor voltage of one cell is the input voltage to the next cell the cell voltage variations are going to accumulate across the chain. This limits the length of the converter chain.

4 Experimental demonstration

To demonstrate the functionality of the proposed converter cell a low voltage, non-optimised prototype was created (fig. 18). A two-cell chain was powered by a 200V DC power supply. Cell capacitances were $C_1 = 220\mu$F and $C_2 = 110\mu$F to simulate the effect of paralleling of two PN cells in the first block of the converter chain, as shown in fig. 17. A modulation index of 0.68 was used for both cells

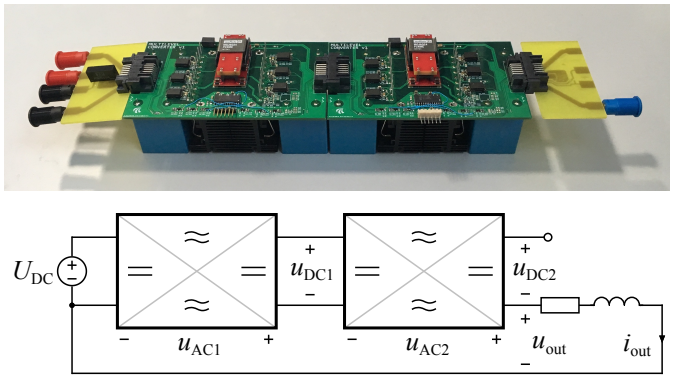

Fig. 18: Proof of concept demonstrator comprised of two daisy-chained converter cells and experimental topology.

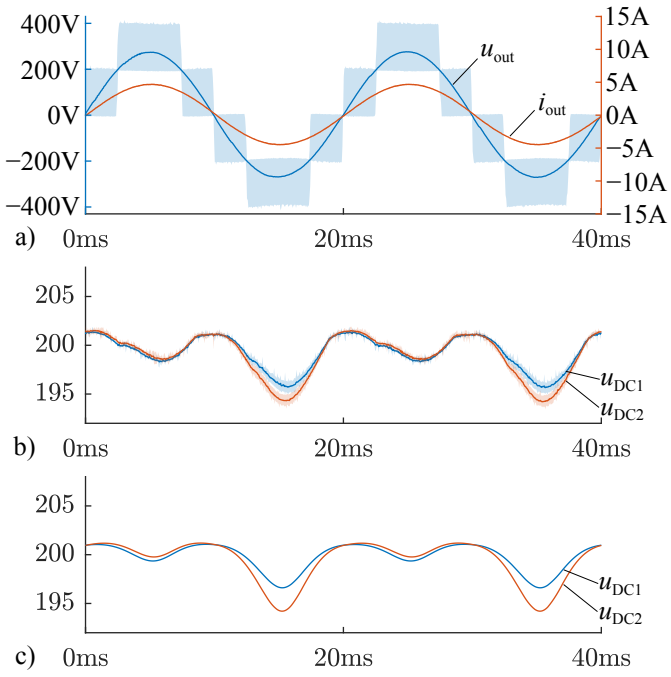

Fig. 19: Key converter waveforms when operating with resistive load ($z = 58\Omega\angle 1.9°$). Solid lines represent the demodulated waveforms:
a measured output current and voltage;
b measured cell capacitor voltages;
c simulated cell capacitor voltages.

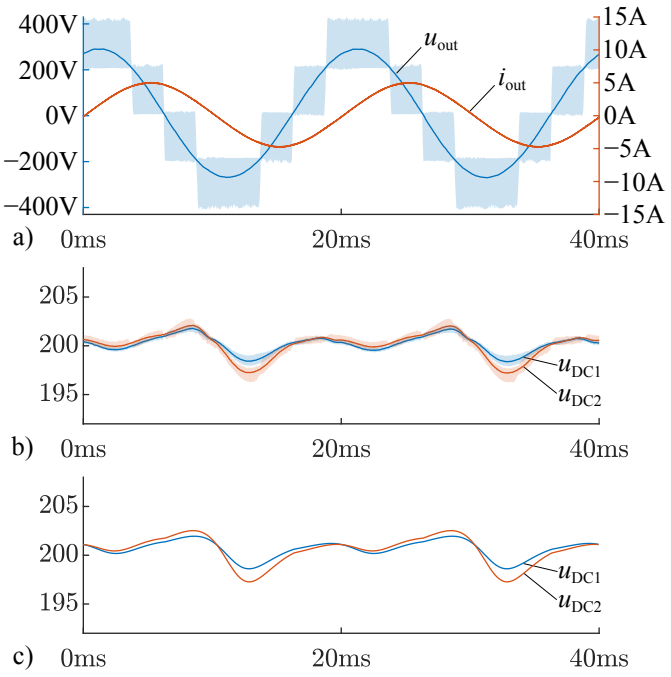

Fig. 20: Key converter waveforms when operating with inductive load ($z = 60\Omega\angle 70°$). Solid lines represent the demodulated waveforms:
a measured output current and voltage;
b measured cell capacitor voltages;
c simulated cell capacitor voltages.

and PWM carriers were shifted by $\pi/4$. SCT3080, SCT3011 and SCT2030 were used as Q_1/Q_3, Q_2/Q_4 and Q_5/Q_6 respectively. 20 kHz switching frequency was used for the demonstrator.

Two experiments were performed: one with resistive load ($R = 58\Omega$, $L = 6mH \rightarrow z = 58\Omega\angle 1.9°$) shown in fig. 19; second with inductive load ($R = 20\Omega$, $L = 180mH \rightarrow z = 60\Omega\angle 70°$) shown in fig. 20. The loads were chosen to yield a similar output current magnitude but at different phase angle.

Results are consistent with the analysis in the previous chapters and closely follow simulated waveforms [17]. As predicted, converter running with inductive load experiences smaller capacitor voltage variation.

5 Related work

As mentioned before in section 2.1, the PN-cell converter is closely related to the CHB topology which is a well known in the high-power industries [15]. The PN cell topology is interestingly also related to low voltage charge pump topologies.

Charge pump converters are a subset of DC/DC converters that use charge stored in capacitors for power conversion. Their key benefit is that they do not utilise magnetic components which can often be bulky. Because of this they are applicable in low power highly integrated circuits. A common application is e.g. level shifting for RS232 communication or generating negative voltage rails. Traditionally they operatie with fixed output/input voltage ratio. Charge pump converters can also operate in power application as e.g. boost converters increasing the input voltage of the source [18].

A subset of charge pump converters family are DC/DC converters that modulate the common mode voltage. During zero common mode voltage state they typically short the cell capacitor to the input voltage thus keeping the DC voltage on the capacitor constant.

He et al. [19] proposed an inverter built by connecting a half-bridge converter to the output of a N-cell. The N-cell can modulate the common mode output (with two states: zero and negative common mode voltage) while providing a DC voltage on the output port. The output voltage from this cell is then modulated by a 2L half-bridge.

Perreault et al. [20] proposed to daisy chain the N-cells to achieve a high voltage conversion ratio between input and output of a converter. With an added active rectifier on the input they created a transformerless AC/DC high input voltage to low output.

Zou et al. [21] presented a full cell switched-capacitor structure where the common mode can have three possible voltage magnitudes (positive, zero and negative). This functionality is inherited by the converter cell presented in this paper as the main principle of operation is identical. The difference lies in implementation of the cell. The presented PN cell merges a P- and N-cell in a single structure. Similar approach is shown also by Vahedi et al. where additional crossover switches are added to increase the number of possible cell levels [22]. In both implementations some of the transistors used in the cell exhibit double the voltage rating of the cell capacitor. In our implementation all transistors are rated only to the cell capacitor voltage.

6 Conclusions

A novel multilevel converter cell is presented that connects a P- and N-cells together yielding a structure capable of generating a three level common-mode voltage and passes a DC voltage between its input and output ports. The DC voltage pass-through allows for an easy daisy chaining of the mentioned cells, generating a multilevel converter structure.

Compared to traditional multilevel converters, with complex control strategies employed to balance the voltages on cell capacitors, the PN converter cell has an intrinsic voltage balancing mechanism. The k-th cell capacitor is charged by shorting it to the $k-1$ cell capacitor. Charging current is limited by the cell switch resistances. The natural voltage balancing scheme has limits, one of the most important one is that it works only during the zero state of the cell thus limiting the maximum modulation index one can use in the converter. Another limitation is that high peak currents are needed to quickly charge the cell capacitance. In practice handling high magnitude peak currents can be expensive because of necessary semiconductor ratings and complex EMC design. By limiting the peak currents we are left with

voltage ripple on capacitor cells that need to be compensated in the control algorithm.

Compared to CHB topology the PN cell based converters do not require a complex one-off transformer to supply the power to individual cells. This makes the system more modular as the power delivery can be done using any industry standard DC topology. This also allows this topology to be used with DC sources such as PV to interface them to the grid.

The PN cell based converter is very well suited to reactive power applications, such as STATCOM systems. Cell capacitor charging is done during the zero switching state (d_0). On the other hand capacitor discharging is the highest during the peak of the chain output current. When handling reactive power the peak converter output current is time-aligned to low cell output voltage when the d_0 is the highest. Due to this alignment cell capacitors experience much lower voltage deviations from nominal than in active power applications.

7 References

[1] Huang, A.Q.: 'Medium-voltage solid-state transformer: Technology for a smarter and resilient grid', *IEEE Industrial Electronics Magazine*, 2016, **10**, (3), pp. 29–42

[2] Rodríguez, J., Bernet, S., Wu, B., et al.: 'Multilevel voltage-source-converter topologies for industrial medium-voltage drives', *IEEE Transactions on industrial electronics*, 2007, **54**, (6), pp. 2930–2945

[3] Wang, F., Zhang, Z., Ericsen, T., et al.: 'Advances in power conversion and drives for shipboard systems', *Proceedings of the IEEE*, 2015, **103**, (12), pp. 2285–2311

[4] Qashqai, P., Sheikholeslami, A., Vahedi, H., et al. 'A review on multilevel converter topologies for electric transportation applications'. In: 2015 IEEE Vehicle Power and Propulsion Conference (VPPC), 2015

[5] Palmour, J., Cheng, L., Pala, V., et al. 'Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV'. In: 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2014. pp. 79–82

[6] Dekka, A., Wu, B., Fuentes, R.L., et al.: 'Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters', *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2017, **5**, (4), pp. 1631–1656

[7] Lesnicar, A., Marquardt, R. 'An innovative modular multilevel converter topology suitable for a wide power range'. In: 2003 IEEE Bologna Power Tech Conference Proceedings, vol. 3, 2003

[8] Perez, M.A., Bernet, S., Rodriguez, J., et al.: 'Circuit topologies, modeling, control schemes, and applications of modular multilevel converters', *IEEE Transactions on Power Electronics*, 2015, **30**, (1), pp. 4–17

[9] Mittal, N., Singh, B., Singh, S.P., et al. 'Multilevel inverters: A literature survey on topologies and control strategies'. In: 2nd International Conference on Power, Control and Embedded Systems, 2012

[10] Choudhury, A., Pillay, P., Williamson, S.S.: 'Comparative analysis between two-level and three-level DC/AC electric vehicle traction inverters using a novel DC-link voltage balancing algorithm', *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2014, **2**, (3), pp. 529–540

[11] Deng, F., Chen, Z.: 'A control method for voltage balancing in modular multilevel converters', *IEEE Transactions on Power Electronics*, 2014, **29**, (1), pp. 66–76

[12] Sepahvand, H., Liao, J., Ferdowsi, M.: 'Investigation on capacitor voltage regulation in cascaded H-bridge multilevel converters with fundamental frequency switching', *IEEE Transactions on Industrial Electronics*, 2011, **58**, (11), pp. 5102–5111

[13] Khazraei, M., Sepahvand, H., Corzine, K., et al. 'A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters'. In: Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010. pp. 58–62

[14] Merlin, M.M., Green, T.C.: 'Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter', *IET Power Electronics*, 2014, **8**, (3), pp. 350–360

[15] Hammond, P.W.: 'A new approach to enhance power quality for medium voltage AC drives', *IEEE Transactions on Industry Applications*, 1997, **33**, (1), pp. 202–208

[16] Debnath, S., Qin, J., Bahrani, B., et al.: 'Operation, control, and applications of the modular multilevel converter: A review', *IEEE transactions on power electronics*, 2015, **30**, (1), pp. 37–53

[17] Bęczkowski, S., Munk-Nielsen, S.: 'Simulation files for a three-level PN converter cell', DOI:10.6084/m9.figshare.8832332,

[18] Voyer, N., inventor; 'Method and an apparatus for controlling the output voltage of a boost converter', US8873260, 2014

[19] He, X.N., Gu, Y., Li, W.H., et al., inventors; 'Inverter without transformer realised by switched capacitor and applications of inverter', CN102088252B, 2012

[20] Perreault, D.J., Li, W., Salazar, N.J.T., inventors; 'Apparatus for multi-level switched-capacitor rectification and DC-DC conversion'. US9450506, 2016

[21] Zou, K., Scott, M.J., Wang, J. 'Switched capacitor cell based DC-DC and DC-AC converters'. In: Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2011. pp. 224–230

[22] Vahedi, H., Al-Haddad, K., Ounejjar, Y., et al. 'Crossover switches cell (CSC): A new multilevel inverter topology with maximum voltage levels and minimum DC sources'. In: 39th Annual Conference of the IEEE Industrial Electronics Society (IECON), 2013, pp. 54–59